

A Broadband mm-Wave and Terahertz Traveling-Wave Frequency Multiplier on CMOS

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Abstract—A wideband frequency multiplier that effectively generates and combines the even harmonics from multiple transistors is proposed. It takes advantage of standing-wave formation and loss cancellation in a distributed structure to generate high amplitude signals resulting in high harmonic power. Wide bandwidth operation and odd harmonic cancellation around the center frequency are the inherent properties of this frequency multiplier. Using this methodology, we implemented a frequency doubler that operates from 220 GHz to 275 GHz in a standard 65 nm CMOS process. Output power of -6.6 dBm (0.22 mW) and conversion loss of 11.4 dB are measured at 244 GHz.

Index Terms—CMOS, frequency doubler, frequency multiplier, harmonic generation, high power source, loss cancellation, millimeter-wave, negative impedance, nonlinearity, standing wave, sub-millimeter wave, Terahertz, traveling wave, wide bandwidth.

I. INTRODUCTION

TERAHERTZ and high millimeter-wave (mm-wave) frequencies are increasingly used in imaging, spectroscopy, communication and radar systems [1]–[3]. Detection of concealed weapons, cancer diagnosis, semiconductor wafer/device inspection, vehicular radars, and high data rate communication, along with bio/molecular spectroscopy for explosive and illegal drug detection, food quality control, and breath analysis for disease diagnosis are among many applications in these frequency ranges [4]–[8].

High power tunable signal sources are one of the most challenging parts of these systems. Voltage-controlled oscillators (VCO) are widely used as tunable signal sources at lower frequencies. However, at terahertz and high mm-wave frequencies, solid-state VCOs suffer from high phase noise, low output power and low tuning range. This is mainly due to the low quality factor of varactors as well as the poor transistor gain at

these frequencies [9]. To alleviate these drawbacks, frequency multipliers using diodes or transistors are commonly employed. Schottky diode is the most popular device in diode-based frequency multipliers [10]–[18]. Due to its structure it is difficult to integrate Schottky diode with other blocks such as amplifiers and oscillators [19]. Moreover, because of the passive nature of diode-based multipliers, the required input power to push the diodes into the nonlinear region is high and therefore the conversion gain is low for low input power levels. Isolation between input and output is another challenge that needs to be addressed in any diode-based multiplier.

On the other hand, transistor-based multipliers can take advantage of the transconductance of the transistor to boost the voltage swing at input and/or output nodes and therefore increase the conversion gain even at low input power levels. Furthermore, using two-port devices, high input-output isolation can be achieved in these frequency multipliers. Transistor-based multipliers also have the advantage of being easily integrated with other building blocks of the system. This is specially valuable in CMOS as it offers low-cost and reliable fabrication of various analog and digital blocks. CMOS frequency multipliers have been proposed for frequencies below 150 GHz [9], [14]–[17], [20]. At higher frequencies, multipliers are implemented using III-V-based transistors or silicon-based HBTs [19], [21]–[24]. Recently, CMOS harmonic VCOs have also been introduced for signal generation at these frequencies [25]–[27]. However, as discussed, the output power and tuning range is too low to be useful in real applications.

In this paper we introduce a novel wideband frequency multiplier that can effectively generate and combine harmonics in order to achieve high output power at high mm-wave and terahertz frequencies [28]. Using this methodology, a frequency doubler that operates from 220 GHz to 275 GHz was implemented in a 65 nm CMOS process. Output power of 220 μ W (-6.6 dBm) and conversion loss of 11.4 dB are achieved at 244 GHz. To the best of our knowledge, this work has twice the operating frequency and tuning range of the fastest CMOS multiplier and has higher output power than any CMOS signal source in this frequency range. The performance of the frequency doubler is comparable with monolithic compound semiconductor frequency multipliers.

The rest of this paper is organized as follows. In Section II, we describe the basic idea and the design procedure of the proposed frequency multiplier. The design, simulation, and measurement

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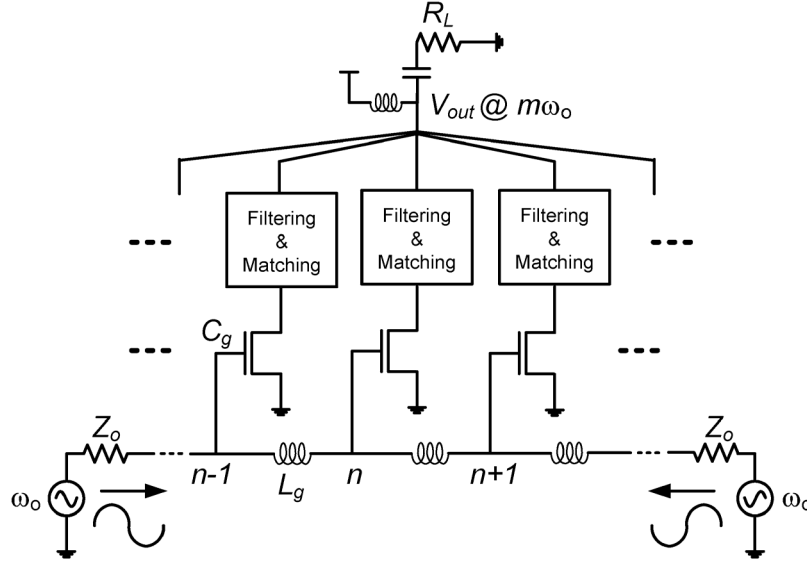


Fig. 1. Schematic of the traveling-wave frequency multiplier.

procedure and results of the implemented frequency doubler are discussed in Section III. We summarize the paper in Section IV.

II. TRAVELING-WAVE FREQUENCY MULTIPLIER

A. The Basic Operation

Fig. 1 shows the basic idea of the proposed frequency multiplier. The input network is an N -section discrete transmission line which is formed by transistor gate capacitors, C_g , and line inductors, L_g . Two signal sources with the same frequency, ω_o , are connected to two ends of this transmission line. The two signals travel in opposite directions and their superposition is applied to the gate of the transistors. Due to nonlinearity, the drain currents contain the harmonics of the input signal. The filtering and matching blocks select the desired harmonic and match the transistors to the load, R_L . Although CMOS transistors are shown in Fig. 1 as the nonlinear components, any nonlinear device including one-port devices such as varactors or diodes can be used to implement this frequency multiplier. More nonlinear devices such as HBTs would result in stronger harmonic generation and higher output power.

Here we assume the loss of the transmission line is negligible. In Section III-A, we justify this assumption by demonstrating how to cancel most of the loss by creating negative impedance using transistors. With this assumption, the voltage at node n is derived to be

$$V_n(t) = A \cos(\omega_o t - kn) + A \cos(\omega_o t - k(N - n) - \phi) \quad (1)$$

where A is the voltage amplitude of the input sources, N is the number of sections, ϕ is the phase difference between the two signal sources, and k is the signal phase shift per section of the transmission line and is defined as

$$k = \omega_o \sqrt{L_g C_g}. \quad (2)$$

We can model the nonlinearity of the transistors by

$$I_{d_n}(t) = a_1 V_n(t) + a_2 V_n^2(t) + a_3 V_n^3(t) + a_4 V_n^4(t) \cdots \quad (3)$$

where $I_{d_n}(t)$ is the n th transistor drain current and the a_k 's ($k \geq 2$) are the nonlinearity coefficients, which are usually a function of transistor bias point, input signal amplitude, and frequency [29]. By substituting (1) in (3), the nonlinearity terms of (3) can be expanded to be

$$a_1 V_n(t) = 2a_1 A \cos\left(\frac{1}{2}kN + \frac{1}{2}\phi - kn\right) \times \cos\left(\omega_o t - \frac{1}{2}kN - \frac{1}{2}\phi\right), \quad (4a)$$

$$a_2 V_n^2(t) = a_2 A^2 [\cos(kN + \phi - 2kn) + 1] \times \cos(2\omega_o t - kN - \phi) + B, \quad (4b)$$

$$a_3 V_n^3(t) = a_3 A^3 \left[\frac{3}{2} \cos\left(\frac{1}{2}kN + \frac{1}{2}\phi - kn\right) + \frac{1}{2} \cos\left(\frac{3}{2}kN + \frac{3}{2}\phi - 3kn\right) \right] \times \cos\left(3\omega_o t - \frac{3}{2}kN - \frac{3}{2}\phi\right) + C, \quad (4c)$$

$$a_4 V_n^4(t) = a_4 A^4 \left[\cos(kN + \phi - 2kn) + \frac{1}{4} \cos(2kN + 2\phi - 4kn) + \frac{3}{4} \right] \times \cos(4\omega_o t - 2kN - 2\phi) + D \quad (4d)$$

where B is the summation of all the DC components, C is the summation of the DC and fundamental components and D is the summation of the DC and second harmonic components. All the harmonics are in phase from different transistors because their phases are not a function of node number, n . However the signal amplitudes are a function of n and hence may not be the same at different nodes. It is clear from (4) that the odd harmonics can have positive and negative amplitudes at different nodes and this will result in destructive power combining. On the other hand, the amplitudes of even harmonics are always positive at different nodes and hence add up constructively in an ideal power

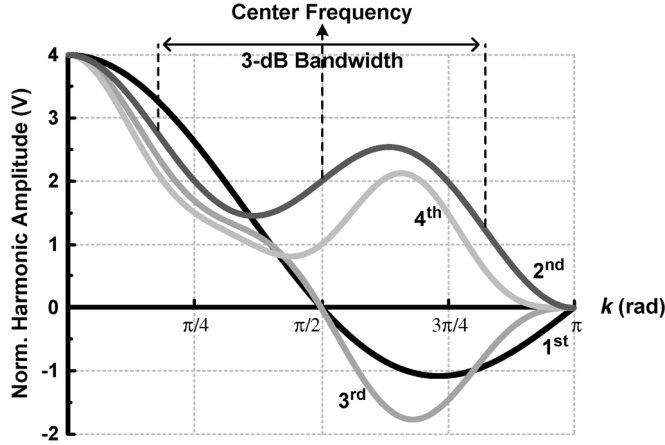


Fig. 2. Normalized harmonic amplitudes in a two-stage multiplier as a function of the wavenumber, k .

combiner. Similarly, by expanding other terms of (3), it can be shown that all the other even harmonics (6th, 8th, etc.) are always in phase from all the transistors.

Due to frequency independent phase matching, this frequency multiplier has the potential to achieve wide bandwidth and high output power at the same time. Using an ideal power combiner (e.g., putting an antenna at the output of each transistor and add the signals spatially) we can add the output power of all the sections for all the frequencies. Compared to a conventional frequency multiplier (e.g., stand-alone transistor) this frequency multiplier takes advantage of standing wave formation at the gate of the transistors and increases the voltage swing. Doing so we can achieve high power harmonic generation and wide bandwidth operation at the same time. This standing-wave is created by the counter-propagating signals along the input transmission line. As will be discussed in Section II-B, this structure also cancels the odd harmonics around the center frequency which results in a cleaner output spectrum.

Using (4), we plot the normalized harmonic amplitudes in a two-stage multiplier (i.e., $N = 2$) as a function of k (i.e., frequency) in Fig. 2. Each harmonic amplitude is normalized to its own nonlinear coefficient, a_k . In this simulation we assume $A = 1$, $k = \phi$ and the transistors are placed at nodes $n = 0$ and $n = 1$. We will discuss the importance of these conditions in Sections II-B and II-C. In this simulation we use an ideal power combiner to add the signals from both transistors. For example, using (4b) the plotted normalized amplitude of the second harmonic is $\cos(2k + k) + 1 + \cos(2k + k - 2k) + 1$. According to Fig. 2, if the center frequency is placed at $k = \pi/2$, a wide bandwidth for even harmonics and odd harmonic cancellation around the center frequency is achieved. For example, if we assume the center frequency at $k = \pi/2$, the input 3-dB bandwidth for the second harmonic is calculated to be $1.27\omega_0$ which translates to 127% 3-dB tuning range at input and output.

B. Odd Harmonic Cancellation

In order to cancel the odd harmonics at the output we need to find the conditions for k and ϕ . One way to do this is to find the conditions in which the amplitudes of all the odd harmonics are zero at all the nodes (e.g., $\cos((1/2)kN + (1/2)\phi - kn) =$

0). However, this is not a useful state because this also means that the output amplitude and hence the input amplitude of the fundamental frequency is zero at all the nodes. The zero input voltage at fundamental results in zero even harmonics at the output. An example of this condition can be viewed in Fig. 2 at $k = \pi$.

The other way to cancel the odd harmonics is for any stage to cancel the odd harmonics of its adjacent stage. In this method, a total odd harmonic cancellation happens at the output only if the number of stages, N , is even. From (4a) we can derive the condition for cancellation of the fundamental component to be

$$\begin{aligned} \cos\left(\frac{1}{2}kN + \frac{1}{2}\phi - kn\right) &= -\cos\left(\frac{1}{2}kN + \frac{1}{2}\phi - k(n+1)\right) \\ \Rightarrow k &= \pi \quad \text{OR} \quad k(N - 2n - 1) + \phi = \pi. \end{aligned} \quad (5)$$

Two of the solutions for the above equation are $k = \pi$ and $k = 0$ which are not acceptable: $k = 0$ means that the phase shift per section is zero and is impractical in Fig. 1. $k = \pi$ implies the 180° phase shift per section which occurs at the cut-off frequency of the line and again is not feasible. It is impossible to find an acceptable solution for all n 's and all even N 's. Therefore, we find the solutions of (5) for four different cases:

$$N=2, 6, 10, \dots \quad \& \quad n=\text{even} \Rightarrow k=\pi/2 \quad \& \quad \phi=\pi/2, \quad (6a)$$

$$N=2, 6, 10, \dots \quad \& \quad n=\text{odd} \Rightarrow k=\pi/2 \quad \& \quad \phi=3\pi/2, \quad (6b)$$

$$N=4, 8, 12, \dots \quad \& \quad n=\text{even} \Rightarrow k=\pi/2 \quad \& \quad \phi=3\pi/2, \quad (6c)$$

$$N=4, 8, 12, \dots \quad \& \quad n=\text{odd} \Rightarrow k=\pi/2 \quad \& \quad \phi=\pi/2. \quad (6d)$$

These are the conditions in which the fundamental component is canceled at the output of the multiplier. Similarly, it is easy to show that the same solutions in (6) will result in all the other odd harmonics to cancel out at the output. The solution of $k = \pi/2$ is practical to implement in Fig. 1 and ensures that the center frequency is well below the cut-off of the line. If we have a two-stage multiplier with $k = \phi = \pi/2$, based on (6a) the transistor at node $n = 0$ ($n = 2, \dots$) will cancel the odd harmonics of the transistor at node $n = 1$ ($n = 3, \dots$). That is why in Section II-A we chose $k = \phi$ and put the transistors at nodes $n = 0$ and $n = 1$ to perform the simulation. Fig. 2 verifies that the odd harmonics are canceled at $k = \phi = \pi/2$.

C. Power Combining

Although the even harmonic components are in phase from different transistors, their amplitudes, as shown in (4), are a function of the node number, n , and may not be equal. The unequal harmonic amplitudes are the direct result of unequal standing wave amplitudes at the gate of the transistors. If we use the power combiner in Fig. 1 the unequal even harmonic amplitudes result in an inefficient power combining. Therefore we need to design k and ϕ in order to have the same gate voltage amplitude for all the transistors. Using (4b), this translates to

$$\begin{aligned} \cos(kN + \phi - 2kn) &= \cos(kN + \phi - 2k(n+1)) \\ \Rightarrow (kN + \phi - 2kn) &= \pm(kN + \phi - 2k(n+1)) + 2m\pi \end{aligned} \quad (7)$$

in which m is an integer. The solutions for (7) are derived to be

$$k = m\pi,$$

$$\phi = k(2n - N + 1) + m\pi. \quad (8)$$

The first solution can be expanded to two unique solutions of $k = 0$ and $k = \pi$ which are not acceptable as discussed. The second solution may be acceptable but the problem is that k and ϕ are a function of n which is variable. In order to have constant values for k and ϕ we expand the second solution for when N is even and odd:

$$N = \text{even} \Rightarrow k = \pi/2 \quad \& \quad \phi = \pm\pi/2,$$

$$N = \text{odd} \Rightarrow k = \pi/2 \quad \& \quad \phi = m\pi. \quad (9)$$

These are the conditions in which the second harmonic components have the same amplitude from different transistors. Similarly, it is easy to show that the same solutions in (9) will result in all the other even harmonics to have the same amplitude from different transistors. Combining (6) and (9) we have the tools to design a multiplier using the topology in Fig. 1.

It is noteworthy that as we move away from the center frequency in which (9) is satisfied, the power would not add up efficiently in Fig. 1 and as a result the bandwidth drops compared to the simulation shown in Fig. 2. However, the odd harmonic cancellation conditions in (6) are general and is valid for any kind of power combiner including the one shown in Fig. 1.

Since the desired harmonics are in-phase at the output, a simple low-loss power combining network can be used to add the power. To ensure the same distance from each transistor to the load, a tree structure or a circular geometry can be used, as shown in Fig. 3. This is a similar frequency multiplier as in Fig. 1 with four sections. The only difference is that the inputs are connected together to make a single-input multiplier. The input signal is applied to the bottom of the structure and divides into two identical parallel paths and reflects back at point “A” which is the common-mode node for the input signal. The phase shift between the counter-propagating signals is designed to satisfy (6) and (9). The main advantage of the circular structure is that it enables us to realize the circuit using only one input that guarantees the frequency matching between the two traveling waves, as well as lower chip area. Furthermore, it minimizes the length of the output power combiner, which means lower loss at the high output frequency.

III. A 220 GHz TO 275 GHz FREQUENCY DOUBLER

A. Design and Simulation

Fig. 4 shows the CMOS implementation of the proposed frequency multiplier with four sections. The input matching network consists of C_{in} and L_{in} and the output matching network is constructed using L_d and C_d . As discussed, the incident wave travels from the signal source at the bottom of the structure and reflects back at point “A”. To better illustrate the operation of the circuit in this example, the half circuit of the input network is shown in Fig. 5. Assuming a good input matching, the voltages at different nodes are constructed by the superposition of the incident and reflected waves as shown in this figure. Here k is the wavenumber which is the phase shift per section and

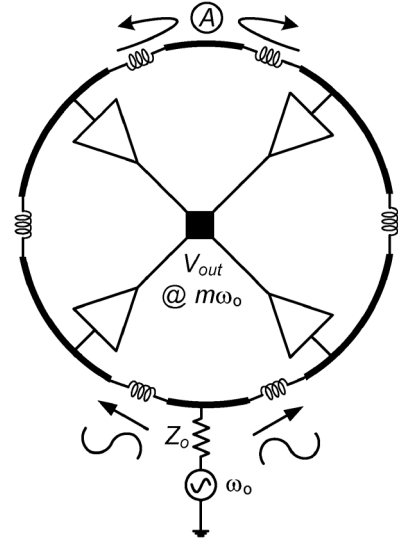


Fig. 3. Circular geometry for the frequency multiplier.

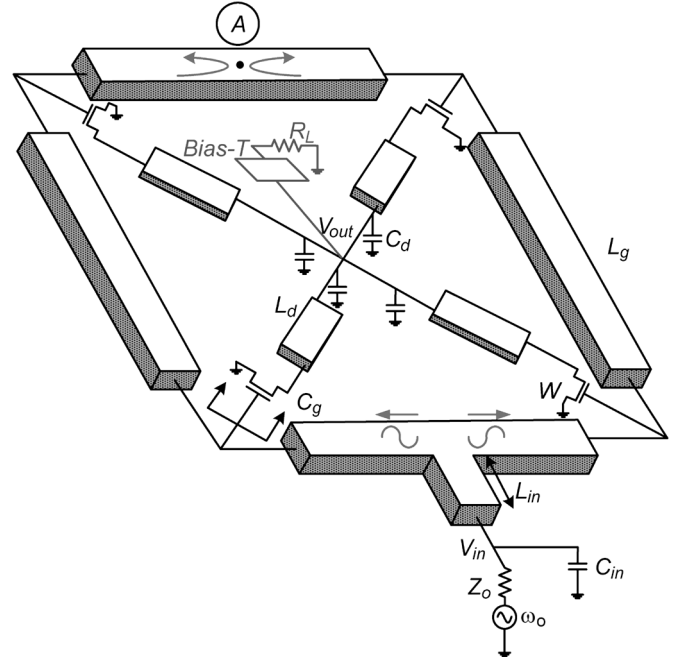


Fig. 4. Circuit implementation of the proposed frequency multiplier.

is defined by (2) and ϕ is the phase shift of the signal when it travels and reflects back through the last half-inductor, $L_g/2$. Due to zero phase shift of the signal at the end of this half inductor, ϕ is equal to k . Comparing the node voltages in Fig. 5 with (1) it is verified that ϕ is the phase shift between the incident and reflected waves and the two transistors are at nodes $n = 0$ and $n = 1$. According to (6a) and (9) if we design the transmission line to have $k = \phi = \pi/2$ at center frequency, we achieve effective even harmonic power combining and odd harmonic cancellation at the same time. The resulting second harmonic components at center frequency is shown at the output of the transistors in Fig. 5.

A standard 65 nm CMOS process with a top metal thickness of $1.3 \mu\text{m}$ was used to implement the multiplier. The input

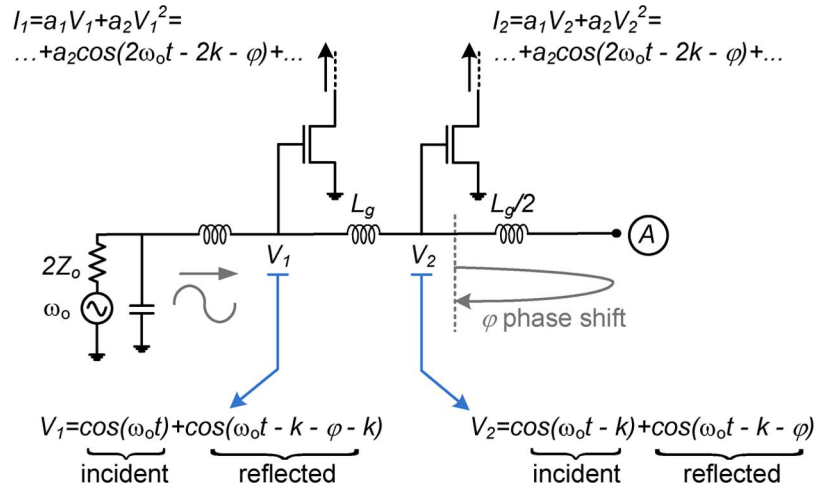
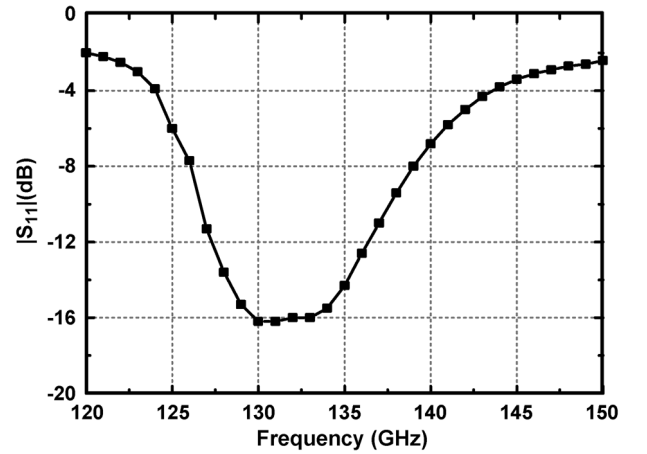


Fig. 5. Half circuit of the input network of the frequency multiplier.

frequency for this prototype is selected to be from 120 GHz to 150 GHz because of available measurement instruments for signal generation, coupling and detection. The second harmonic is selected at the output for higher power generation. Therefore the output matching network is designed to operate from 240 GHz to 300 GHz. All the inductors and capacitors in this frequency doubler are realized using microstrip transmission lines and metal-to-metal capacitance of the probing pads, respectively. The Sonnet electromagnetic simulator was used to design all the passive components [30]. Since for strong harmonic generation high input power is applied to the doubler, the input matching should be designed for large signals. Fig. 6 shows the simulated input reflection coefficient for an input power of 3 dBm. In this simulation $L_g = 60$ pH is implemented using a microstrip transmission line with an electrical length of $\lambda/5$ and quality factor of 13 at 135 GHz. This short electrical length enables us to use this transmission line as an inductor in the circuit. The transistor size of $W = 28 \mu\text{m}$ corresponding to $C_{gd} = 55$ fF are also used for this simulation. These component values result in $k \simeq \pi/2$ at the center frequency of 135 GHz. This k value along with $\phi = k$ which is a direct outcome of the topology satisfy the conditions in (6a) and (9). The L_g and C_g values are also designed to have good matching at the input.

The output impedance is matched to a 50Ω load at $2\omega_0$ using L_d and C_d . Because the output matching network is matched at $2\omega_0$ it appears as an inductive load for the transistor at ω_0 . Under specific conditions the real impedance looking into the gate of a transistor with an inductive load is negative. This negative impedance can be used to cancel most of the loss of the input line, increasing the voltage swing at ω_0 and hence creating significantly stronger harmonic power. Fig. 7(a) shows the equivalent circuit of one section of the frequency doubler which can be used to find the gate input impedance at ω_0 . Since the fundamental frequency is canceled out at the output, it is assumed to be grounded at this frequency. To find the condition for loss cancellation the real part of the input admittance is derived to be

$$\text{Real}[Y_{\text{in}}] = \frac{\frac{C_{gd}g_m}{L_d} \left[L_d \omega_0^2 \left(C_{gd} + C_{ds} + \frac{C_{gd}}{R_o g_m} \right) - 1 \right]}{1/R_o^2 + \left[\omega_0 (C_{gd} + C_{ds}) - \frac{1}{\omega_0 L_d} \right]^2} \quad (10)$$


 Fig. 6. Simulated large-signal input reflection coefficient (S_{11}) of the frequency doubler.

where C_{gd} is the gate-drain capacitor, g_m is the transistor transconductance, and C_{ds} and R_o are the drain-source capacitor and resistor, respectively. Since the denominator in (10) is positive, the real part of the input impedance (or admittance) is negative if

$$L_d \omega_0^2 \left(C_{gd} + C_{ds} + \frac{C_{gd}}{R_o g_m} \right) < 1. \quad (11)$$

The gate resistance of the transistor is not included in deriving the input impedance. Therefore to get an actual negative resistance from the transistor the gate resistance should be compensated. To see the effect of all the losses in the transistor, the real input impedance is simulated as a function of input frequency and L_d in Fig. 7(b). As verified by (10), Fig. 7(b) shows that when the real part of the input impedance is around zero, lower frequency or lower L_d create a larger negative input resistance. There is a trade-off between harmonic matching at the output and loss cancellation at the input. Larger L_d creates a better output matching at the second harmonic but it also reduces the negative input impedance which in turn reduces the gate voltage swing and hence weaker harmonic generation. Optimum values for maximum output power are found to be $L_d = 53$ pH and

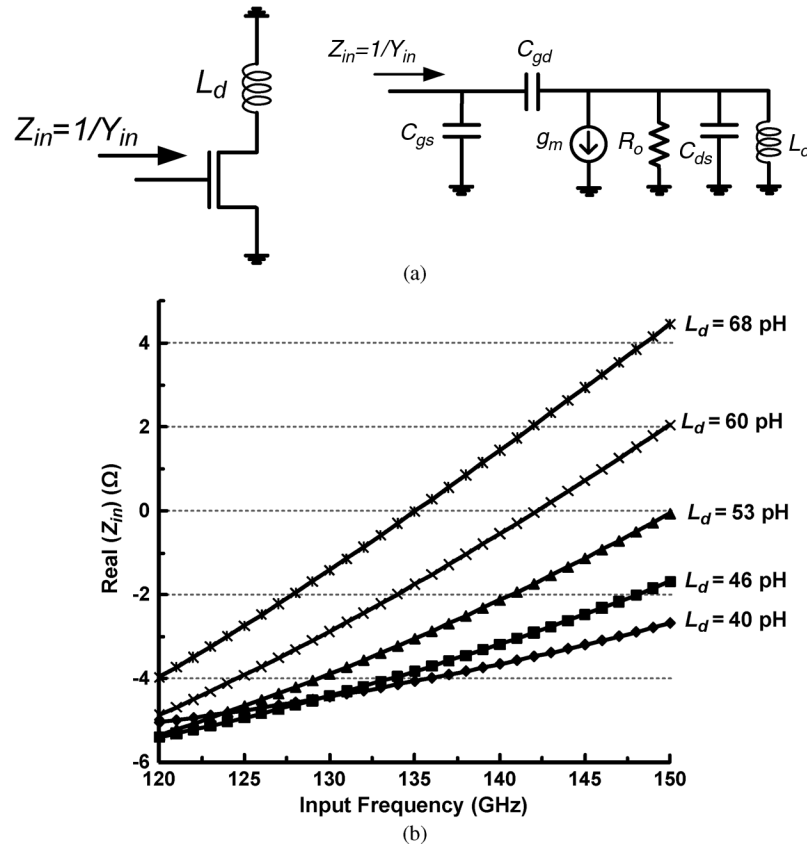


Fig. 7. (a) Equivalent circuit to find the input impedance at ω_0 and (b) the simulated real part of the input impedance as a function of input frequency and L_d .

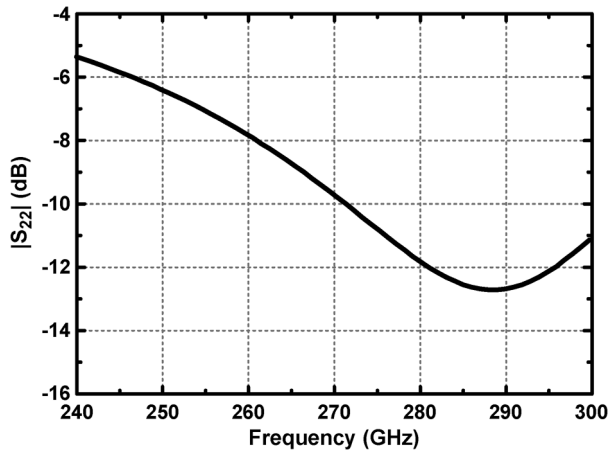


Fig. 8. Simulated output reflection coefficient (S_{22}) of the frequency doubler.

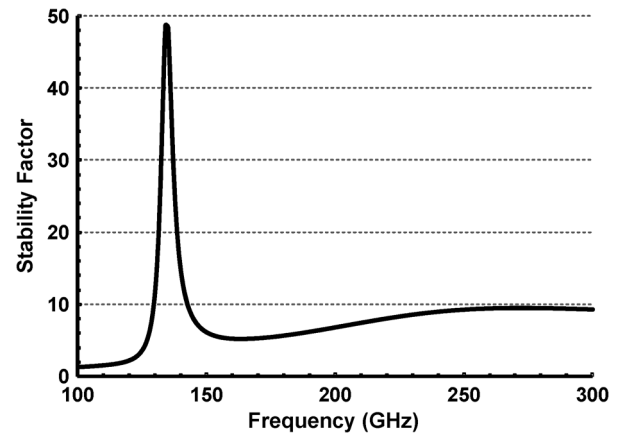


Fig. 9. Stability factor (K-factor) of the frequency doubler as a function of frequency.

$C_d = 8$ fF. These values are also selected to make the doubler unconditionally stable for all the frequencies above 80 GHz. Below 80 GHz the circuit is not unconditionally stable, however, it is stable with 50Ω source and load impedances. At 270 GHz, the quality factor of L_d and C_d are 15 and 80, respectively. Fig. 8 and Fig. 9 show the doubler's simulated output reflection coefficient and stability factor (K-factor), respectively.

Fig. 10 shows the simulated output power and conversion loss as a function of output frequency. In this simulation the input power is kept constant at 3 dBm at ω_0 . The peak output

power and conversion gain occurs at 270 GHz. The simulated output power and conversion loss as a function of input power at the center frequency is plotted in Fig. 11. A peak power of 1 dBm (1.3 mW) and a minimum conversion loss of 6 dB are achieved at this frequency. At the peak output power the doubler consumes 35 mW of DC power from a 1.2 V supply and input bias voltage is 1 V. Fig. 12 demonstrates the simulated output spectrum when the input frequency and power are 135 GHz and 5 dBm, respectively. The power of all the other harmonics are at least 13 dB lower than the second harmonic at 270 GHz.

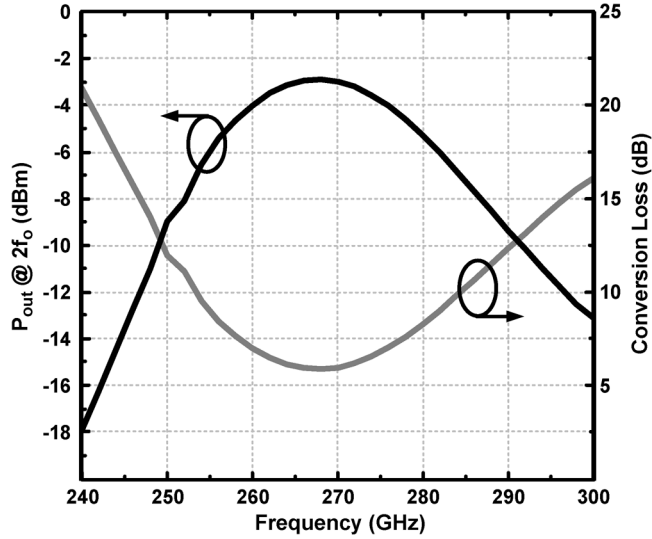


Fig. 10. Simulated output power and conversion loss as a function of output frequency with a constant input power of 3 dBm.

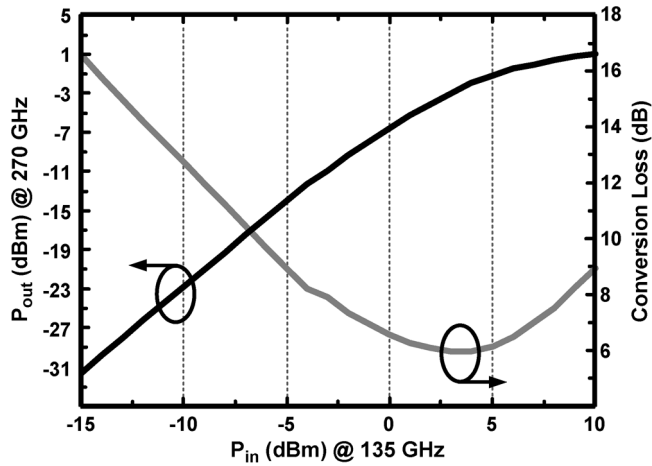


Fig. 11. Simulated output power and conversion loss at 270 GHz as a function of input power.

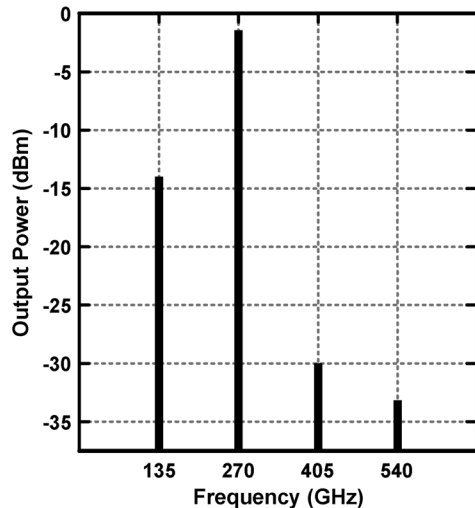


Fig. 12. Simulation of a typical output spectrum when the input frequency and power are 135 GHz and 5 dBm respectively.

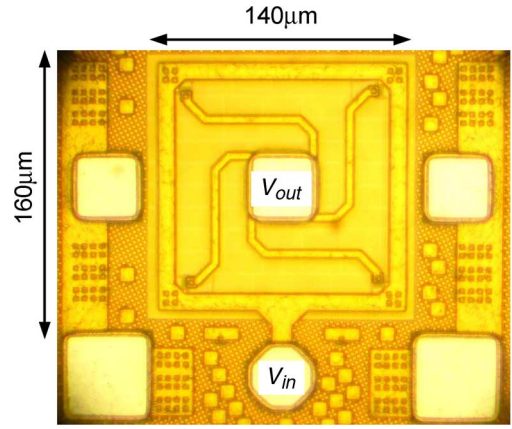


Fig. 13. Die photo of the frequency doubler.

B. Measurement

Fig. 13 shows the die photo of the implemented frequency doubler. As discussed the input and output pads are part of the matching networks. To reduce substrate coupling the entire structure is shielded by a lower metal layer. This structure can be easily wirebonded or flip chipped for external use. Furthermore, an antenna can be implemented at the center of the structure to radiate the power. If an on-chip integration with other blocks are required, a shielded line can be used to guide the signal from the center to the next block. A GGB 140-GSG probe and a Cascade i325-GSG probe with built-in bias tees were used to probe the input and output signals, respectively. The gate bias voltage and the DC supply are provided through the bias tees of the probes. The coupling between the probe and the on-chip transmission lines is minimized by the ground plane which is $6.9 \mu\text{m}$ away from the signal lines. As shown in Fig. 14, two separate setups were used to measure the output frequency and power. Fig. 14(a) shows the frequency measurement setup. A signal generator, an amplifier and a frequency tripler are used to generate the input signal. A harmonic mixer, an LO, and a spectrum analyzer are used to detect the output frequency. The output frequency measurement is limited to the range of 220 to 280 GHz because of the lower and the higher cutoff frequency of the WR-3.0 and the WR-8.0 waveguides, respectively.

With no input signal, no signal was detected at the output or at the input. This means that the circuit is stable and no oscillation happens at the fundamental frequency and above. As the input power reaches -7.4 dBm the output power becomes detectable. By sweeping the LO frequency, f_{LO} , and observing the IF frequency which is $f_{IF} = f_{out} - n f_{LO}$, the LO harmonic number, n , and the signal frequency, f_{out} , can be determined [31]. The detectable output signals from 220 GHz to 275 GHz were measured to have twice the frequencies of the input. A typical measured output spectrum with the 48th harmonic of the LO frequency is shown in Fig. 15. For this spectrum, the input frequency and power are 118.5 GHz and 4.5 dBm, respectively. The loss of the probes and waveguides are characterized using network analyzer by Cascade and GGB and the output power of the VDI frequency tripler is measured using an Erickson PM4 power meter. Therefore, The input power of the implemented frequency doubler can be accurately characterized. Likewise,

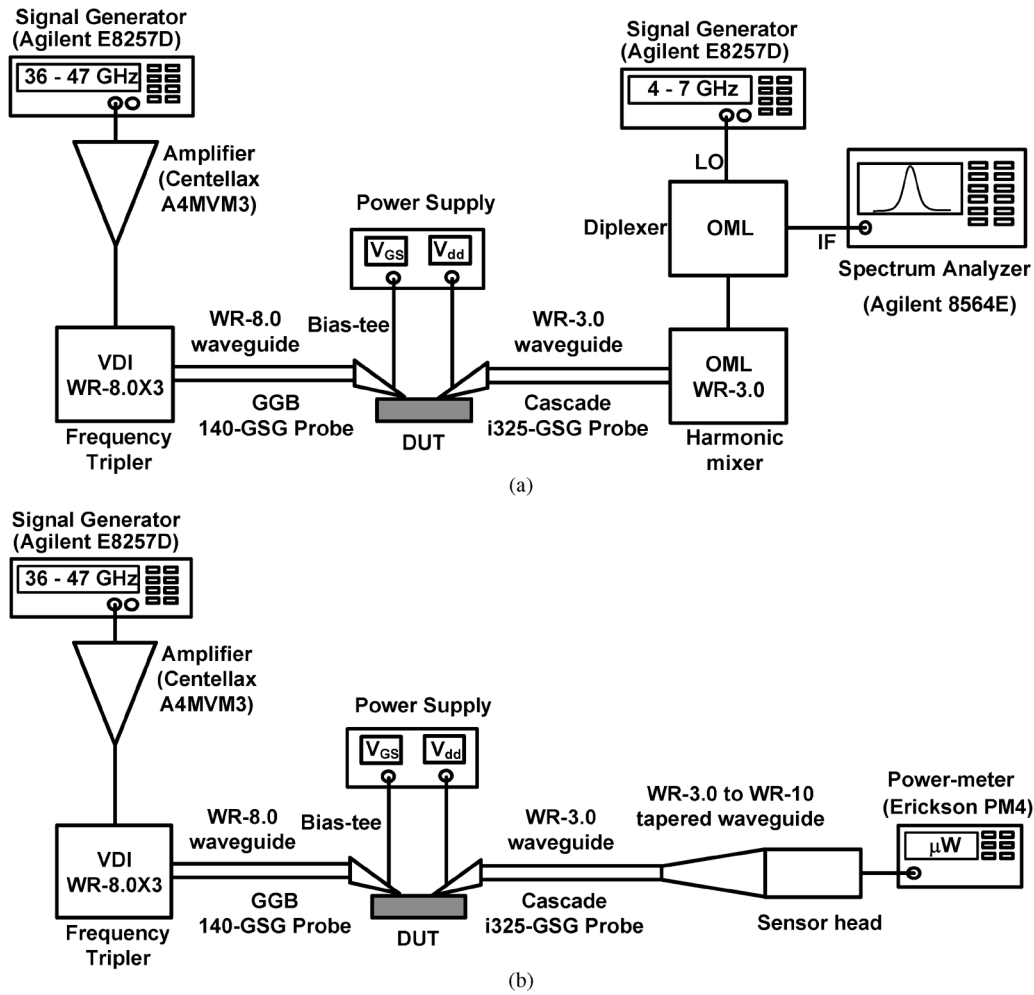


Fig. 14. Test setup for measuring (a) output frequency and (b) output power of the frequency doubler.

having the conversion loss of the OML harmonic mixer the output power of the frequency doubler can be estimated. For the 237 GHz signal in Fig. 15 the loss of the output probe/waveguide and the conversion loss of the mixer for 48th harmonic of the LO frequency are 5 dB and 66 dB, respectively. Given the IF power of -71 dBm the output power is 0 dBm at 237 GHz.

Although the output power can be estimated using harmonic mixers, it is not accurate. This is because harmonic mixers are highly nonlinear devices and it is almost impossible to characterize them for all power levels. To measure the output power accurately we use the setup in Fig. 14(b) with an Erickson PM4 power meter at the output. The power meter works for all the frequencies from 75 GHz to 2 THz and its resolution is 10 nW. A WR-3.0 waveguide which has a pass-band from 220 GHz to 325 GHz is used to direct the signal to the power meter. As a result, all the harmonics below the second harmonic are highly suppressed before the signal reaches the power sensor. As shown in the simulation in Fig. 12, all higher harmonics will either cancel out at the output, have low multiplication efficiency, or will be suppressed by the output matching network. This would result in the power meter readout to be mostly from the second harmonic component. A tapered waveguide is used to make a transition from WR-3.0 to WR-10 which is the waveguide dimension for the power sensor head.

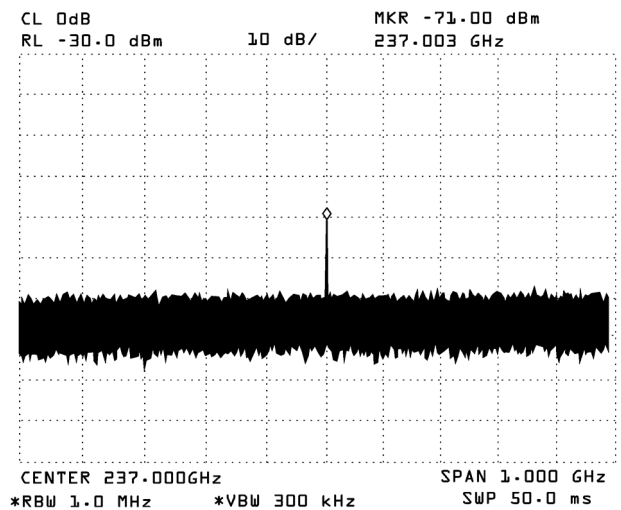


Fig. 15. Measured output spectrum with the input power of 4.5 dBm at 118.5 GHz.

Fig. 16 shows the measured output power and conversion loss as a function of output frequency. In this measurement the input power is kept constant at 3 dBm for all frequencies. This

TABLE I
COMPARISON WITH PRIOR ART

Ref.	This work	[9]	[14]	[26]	[32]	[3]	[24]	[21]	[12]
Frequency (GHz)	244	115	125	324	291	482	225	300	356
Tuning Range	22.2%	13.1%	12.7%	1.2%	NA	NA	17.7%	NA	11.7%
3-dB BW	7.8%	NA	NA	NA	NA	NA	11%	21.4%	9%
Power (dBm)	-6.6/ 0	-2.6	-1.5	-46	-17 (per element)	-7.9	-1	-6.4	8
Power Measurement	Power meter/ Mixer	Mixer	Mixer	Mixer	Mixer	Power meter	Power meter	Power meter	Power meter
Con. Loss (dB)	11.4	NA	10	NA	NA	NA	1	7.4	6.6
DC Power (mW)	40	12	0	12	18.7	61	630	NA	0
Monolithic Integration?	yes	yes	yes	yes	yes	yes	yes	yes	no
Type	$\times 2$ Traveling wave	$\times 2$ Injection locking	$\times 2$ Schottky diode	Superposition VCO	Push-push Oscillator	Triple-Push Oscillator	$\times 2$ Push-push HBT	$\times 2$ Single transistor	$\times 2$ Schottky diode
Technology	65 nm CMOS	65 nm CMOS	130 nm CMOS	90 nm CMOS	45 nm CMOS	65 nm CMOS	130 nm SiGe	50 nm GaAs mHEMT	GaAs Schottkey
Area ($1000\mu\text{m}^2$)	22.4	26.4	210	37.8	160	7.7	611	375	119

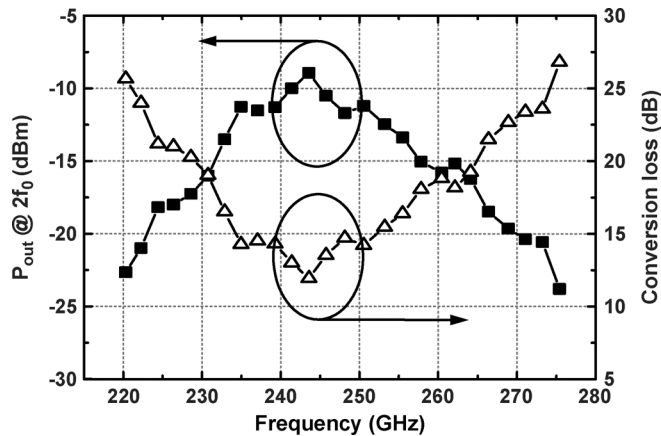


Fig. 16. Measured output power and conversion loss as a function of output frequency using power meter for an input power of 3 dBm.

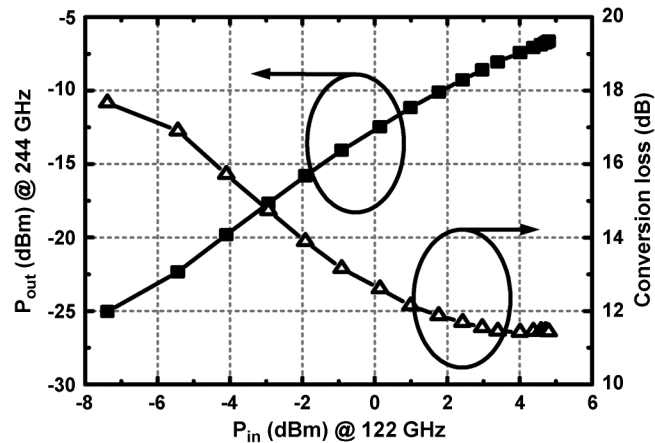


Fig. 17. Measured output power and conversion loss as a function of input power at 244 GHz.

input power level is the highest power that our setup can generate across the entire band. Using this input power, the fre-

quency doubler operates from 220 GHz to 275 GHz. This operating range is limited to the lowest power that can be detected using our equipments. The 3-dB bandwidth of the doubler is from 234 GHz to 253 GHz. The power difference between this measurement and the one from the harmonic mixer is mostly because the mixer is calibrated at lower power levels and the conversion loss values are not valid here. The peak measured power and conversion gain using this setup occurs at 244 GHz. The difference in output frequency range between the simulation and measurement is around 10%. This error is mostly caused by transistor parasitic modeling at this frequency range. Fig. 17 shows the output power and conversion loss as a function of input power at 244 GHz. A peak output power of -6.6 dBm ($220 \mu\text{W}$) with a conversion loss of 11.4 dB is achieved at this frequency. The maximum input power that our setup can provide at 122 GHz is 4.8 dBm and therefore the output power is not saturated as shown in Fig. 17. Given higher input power, we can achieve higher output power. Due to inaccurate modeling of the transistors the measured output power is around 3 dB lower than the simulation which is acceptable for this frequency range. The circuit consumes 40 mW of DC power from a 1.2 V supply.

The comparison with the state of the art is provided in Table I. Compared to reported CMOS frequency multipliers this work has doubled both the operation frequency and tuning range at the same time. Although the output power is not saturated, it is higher than any other CMOS signal source at this frequency range. To have a fair comparison with other CMOS works, the output power is reported using both harmonic mixer and power meter. The doubler's specifications are comparable to monolithic compound semiconductor frequency multipliers.

IV. CONCLUSION

We have proposed a wideband frequency multiplier that effectively generates and combines harmonics from multiple transistors. The experimental results show considerable improvement in the output power and tuning range compared to the state

of the art. The frequency multiplier can be used to replace varactor-based tunable sources in mm-wave and terahertz frequencies for imaging, spectroscopy, communication and radar systems.

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